```
// ***************************************************************************************************************
// **                                                                                                           **
// **   LIN2ALAW.v - LINEAR 2'S COMPLEMENT TO A-LAW CODE TRANSLATOR                                             **
// **                                                                                                           **
// ***************************************************************************************************************
// **                                                                                                           **
// **                              COPYRIGHT (c) 2001 YOUNG ENGINEERING                                         **
// **                                      ALL RIGHTS RESERVED                                                  **
// **                                                                                                           **
// **   THIS PROGRAM IS CONFIDENTIAL AND  A  TRADE SECRET  OF  YOUNG  ENGINEERING.  THE RECEIPT OR              **
// **   POSSESSION  OF THIS PROGRAM  DOES NOT  CONVEY  ANY  RIGHTS TO  REPRODUCE  OR  DISCLOSE ITS             **
// **   CONTENTS,  OR TO MANUFACTURE, USE, OR SELL  ANYTHING  THAT IT MAY DESCRIBE, IN WHOLE OR IN             **
// **   PART, WITHOUT THE SPECIFIC WRITTEN CONSENT OF YOUNG ENGINEERING.                                        **
// **                                                                                                           **
// ***************************************************************************************************************
// **   Revision       : 1.0                                                                                   **
// **   Modified Date  : 11/01/2001                                                                            **
// **   Revision History:                                                                                       **
// **                                                                                                           **
// **   11/01/2001:  Initial design                                                                             **
// **                                                                                                           **
// ***************************************************************************************************************
// **                                        TABLE OF CONTENTS                                                  **
// ***************************************************************************************************************
// **-------------------------------------------------------------------------------------------------------------**
// **   DECLARATIONS                                                                                            **
// **-------------------------------------------------------------------------------------------------------------**
// **-------------------------------------------------------------------------------------------------------------**
// **   FORMAT CONVERSION                                                                                       **
// **-------------------------------------------------------------------------------------------------------------**
// **   1.01:  Input Data Sign Removal                                                                          **
// **   1.02:  Linear to A-Law Table                                                                            **
// **   1.03:  A-Law Output Inversion                                                                           **
// **                                                                                                           **
// ***************************************************************************************************************


`timescale 1ns/10ps

module LIN2ALAW       ( DataI, DataO );

   input  [12:00]       DataI;                          // data input - linear 2's complement

   output [07:00]       DataO;                          // data output - A-Law


// ***************************************************************************************************************
// **   DECLARATIONS                                                                                            **
// ***************************************************************************************************************

   wire [11:00]         LinearData;                     // linear data - unsigned

   reg  [06:00]         A_LawData;                      // A-law encoded data

   wire [07:00]         DataO;                          // data output - A-law


// ***************************************************************************************************************
// **   FORMAT CONVERSION                                                                                       **
// ***************************************************************************************************************
// ---------------------------------------------------------------------------------------------------------------
//      1.01:  Input Data Sign Removal
// ---------------------------------------------------------------------------------------------------------------

   assign LinearData = DataI[12] ? (~DataI[11:00] + 1) : DataI[11:00];

// ---------------------------------------------------------------------------------------------------------------
//      1.02:  Linear to A-Law Table
// ---------------------------------------------------------------------------------------------------------------

   always @(LinearData) begin
      casex(LinearData)
         12'b1xxxxxxxxxxx :     A_LawData = {3'b111,LinearData[10:07]}; // full scale
         12'b01xxxxxxxxxx :     A_LawData = {3'b110,LinearData[09:06]};
         12'b001xxxxxxxxx :     A_LawData = {3'b101,LinearData[08:05]};
         12'b0001xxxxxxxx :     A_LawData = {3'b100,LinearData[07:04]};
         12'b00001xxxxxxx :     A_LawData = {3'b011,LinearData[06:03]};
         12'b000001xxxxxx :     A_LawData = {3'b010,LinearData[05:02]};
         12'b0000001xxxxx :     A_LawData = {3'b001,LinearData[04:01]};
```

```
         12'b0000000xxxxx :     A_LawData = {3'b000,LinearData[04:01]}; // zero point

         default :              A_LawData = {3'b000,LinearData[04:01]};
      endcase
   end

// ------------------------------------------------------------------------------------------------------
//      1.03:  A-Law Output Inversion
// ------------------------------------------------------------------------------------------------------

   assign DataO = {~DataI[12],(A_LawData[06:00] ^ 7'h55)};

endmodule
```